EE2019: Analog Systems and Lab

Course summary

Aniruddhan S
Qadeer Ahmad Khan
Saurabh Saxena

https://courses.iitm.ac.in

Department of Electrical Engineering
Indian Institute of Technology, Madras
Chennai, 600036, India

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RLC circuit analysis

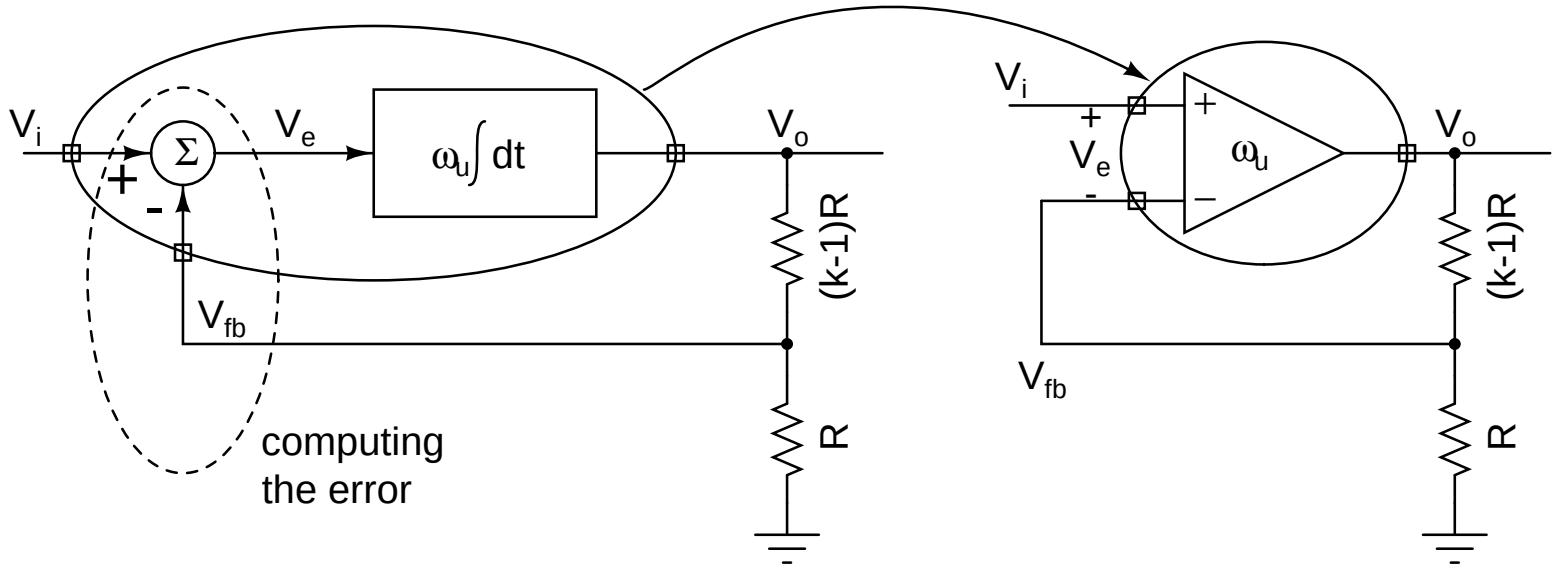
Time domain

- Step response
- Initial/final values and time-constants

Frequency domain

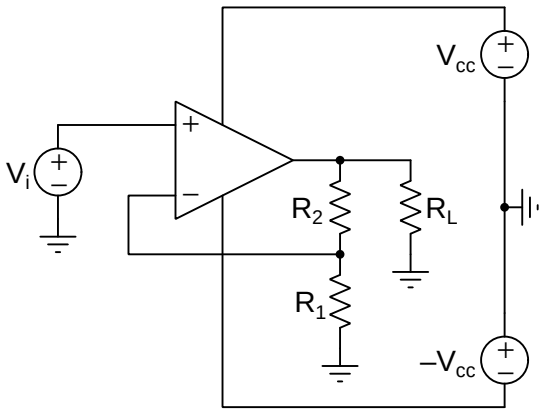
- Transfer function, poles and zeros
- Sinusoidal steady-state response; Bode plots

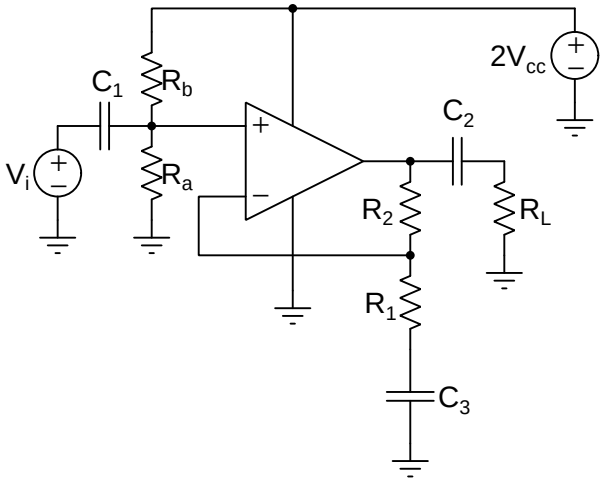
Negative feedback amplifier and the opamp

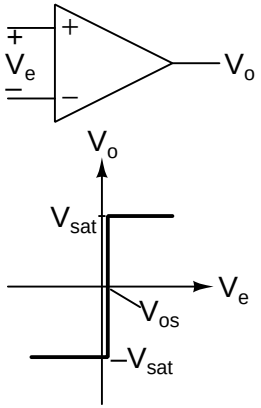


- Infinite gain model
- Virtual short with negative feedback
- Finding opamp signs for negative feedback

Biasing opamp circuits







- Opamp saturation and offset
- Single and dual supply operation
- AC coupling

Opamp characteristics

National Semiconductor

August 2000

LF147/LF347
Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low

Features

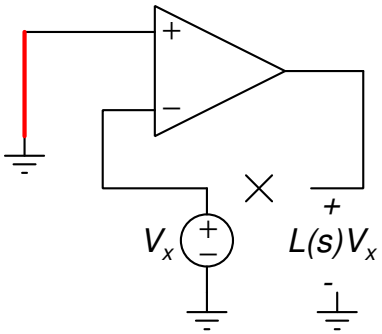
- Internally trimmed offset voltage: 5 mV max
- Low input bias current: 50 pA
- Low input noise current: 0.01 pA/√Hz

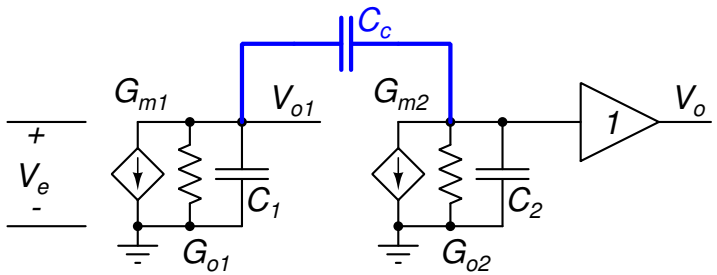
DC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10 kΩ, T_A=25°C		1	5		3	5		5	10	mV
		Over Temperature			8			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10			10			10		µV/°C
I_{OS}	Input Offset Current	T_j=25°C, (Notes 7, 8)		25	100		25	100		25	100	pA
		Over Temperature			25			4			4	nA
I_B	Input Bias Current	T_j=25°C, (Notes 7, 8)		50	200		50	200		50	200	pA
		Over Temperature			50			8			8	nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	50	100		50	100		25	100		V/mV
		V_O=±10V, R_L=2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	R_S≤10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 9)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

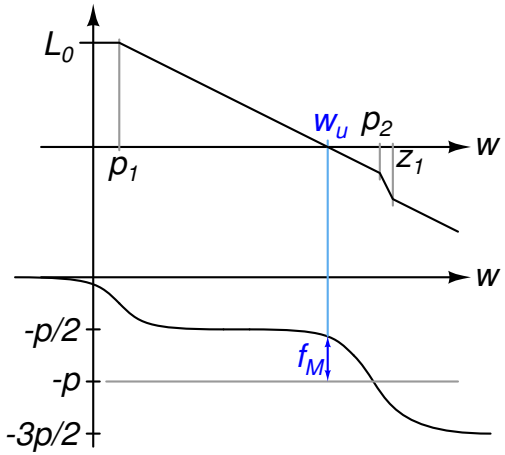
Source: www.ti.com/lit/ds/symlink/lf147.pdf

Stability of negative feedback circuits



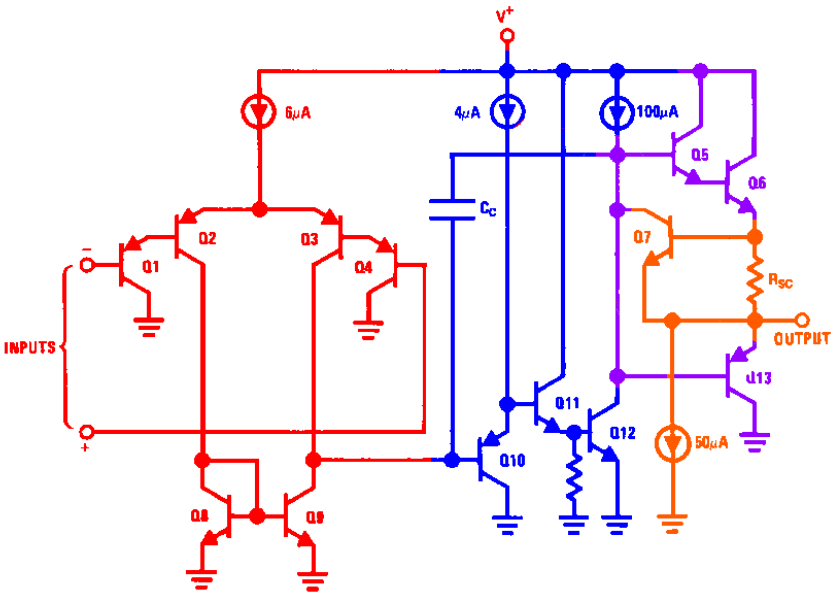


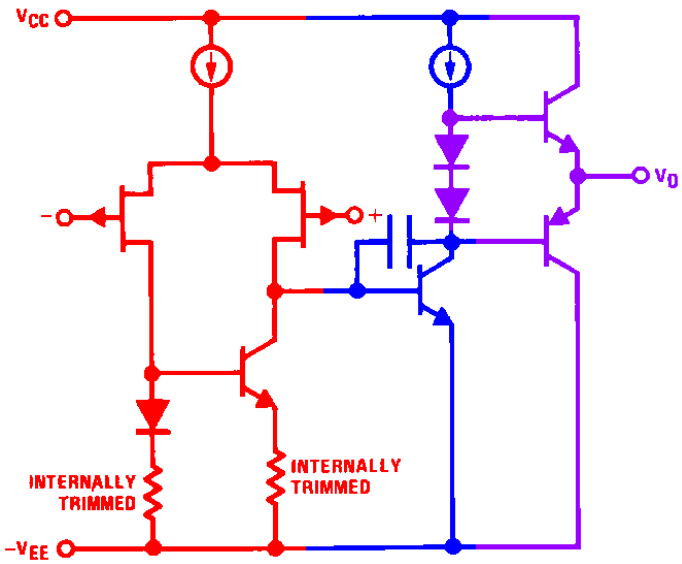
$$L(s) = \frac{L_0(1-s/z_1)}{(1+s/p_1)(1+s/p_2)}$$



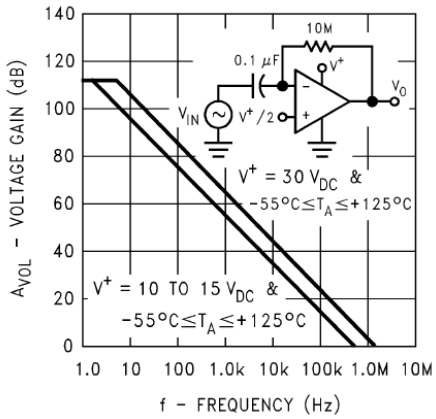
- Stability criterion—Loop gain and phase margin
- Dominant pole compensation
- 2-stage Miller compensated opamp

Opamp examples: LM324, LF147

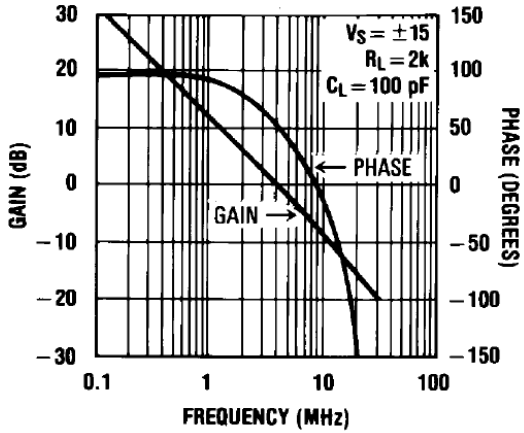




Open Loop Frequency Response



Bode Plot

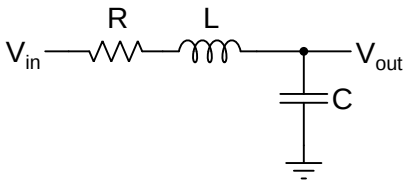


Source: www.ti.com/lit/gpn/lm124, www.ti.com/lit/ds/symlink/lf147.pdf

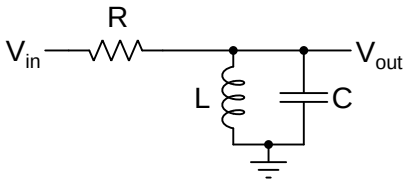
Filters

- Passive RLC filters
- State-variable filter: Emulate equations of RLC filters using integrators
- Sallen-Key, Rauch filters, . . .

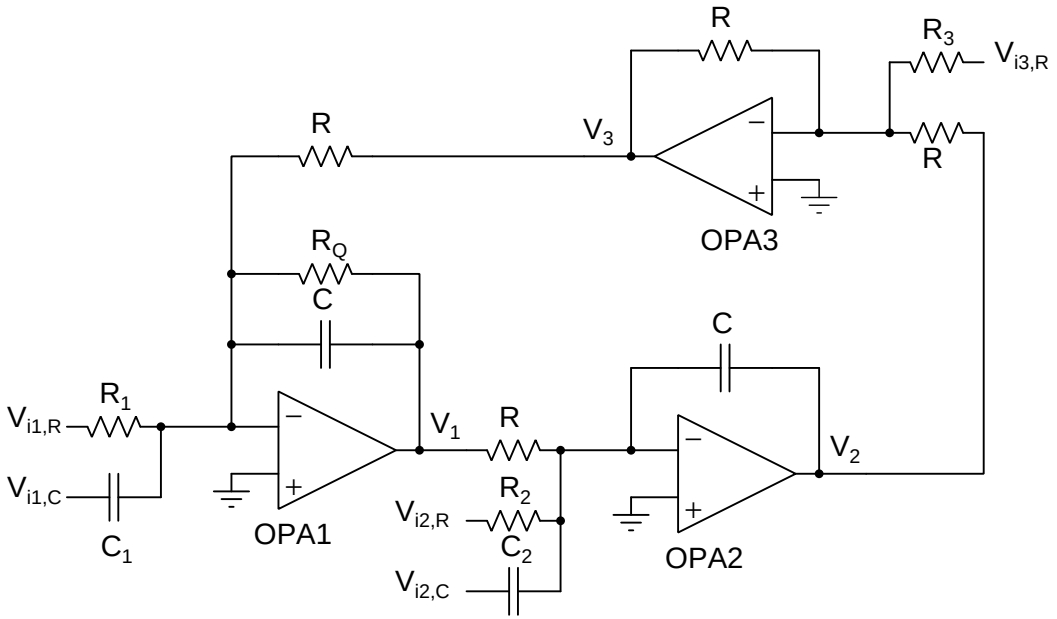
Filters



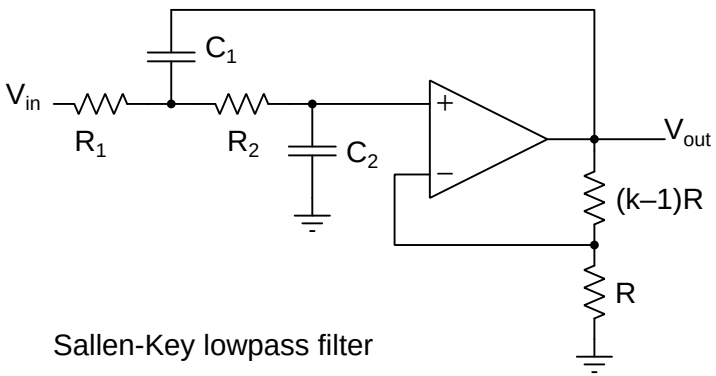
Series RLC lowpass filter



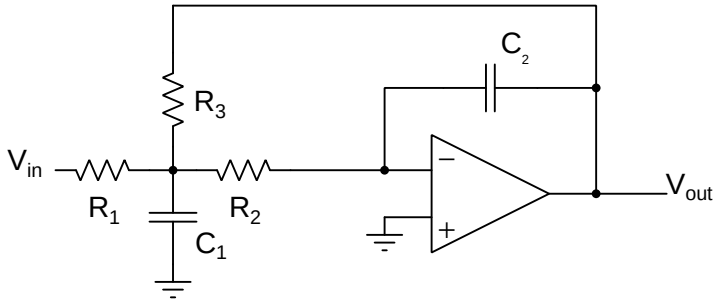
Parallel RLC bandpass filter



Opamp-RC biquadratic filter

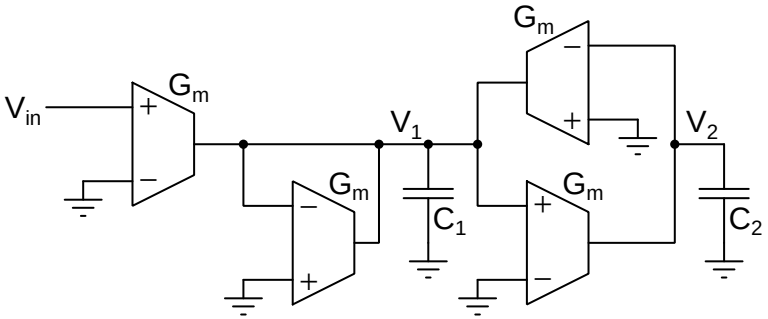


Sallen-Key lowpass filter

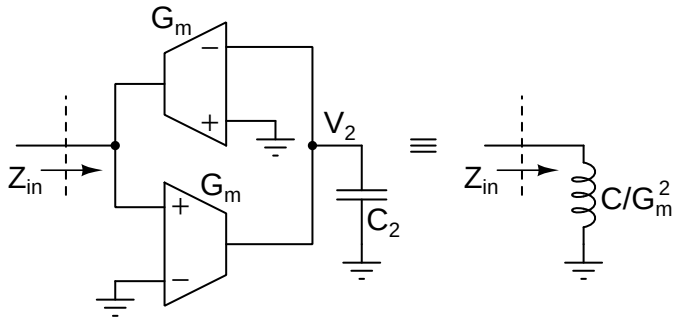


Rauch lowpass filter

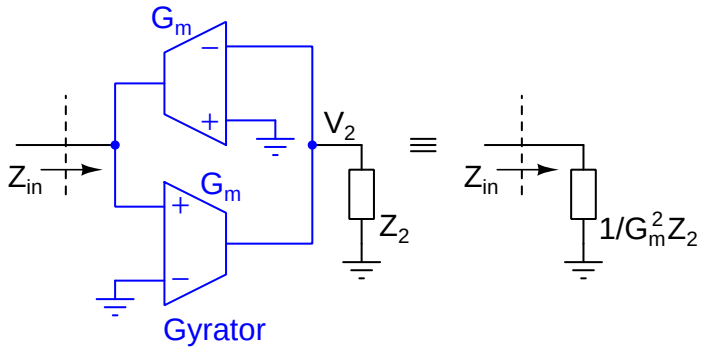
Filters



G_m-C second-order filter



Inductor emulation

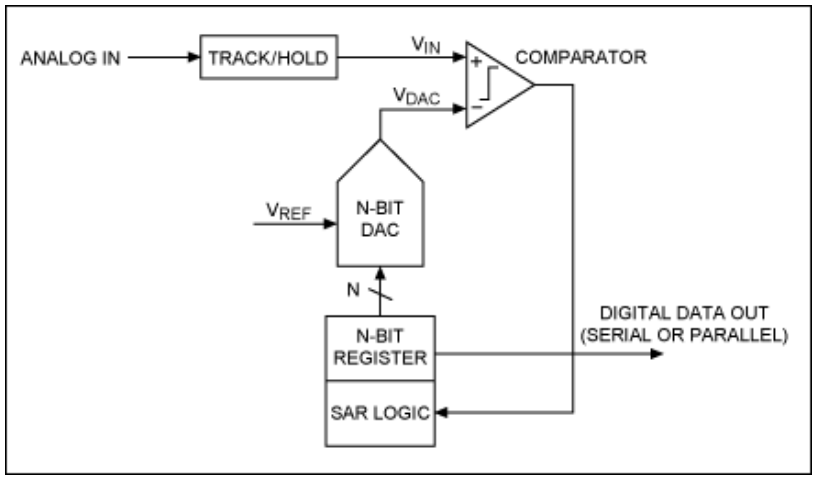


Gyrator

Oscillators

- LC resonant network compensated by a negative conductance
- Wien bridge oscillator
- Schmitt trigger oscillator

Data converters



Sampling

- Track and Hold (T/H), Sample and Hold (S/H)

Analog-to-digital conversion

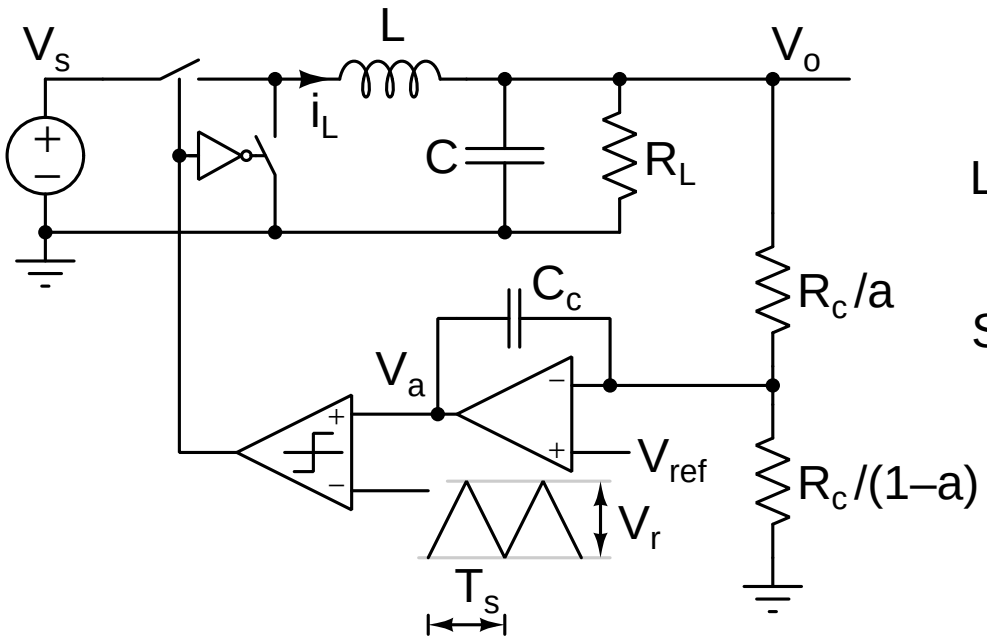
- Flash ADC for high speed and low resolution
- SAR ADC for low speed and high resolution

Digital-to-analog conversion

- Resistor DAC: Resistor string, R-2R, binary weighted
- Binary weighted capacitor DAC (Suited for SAR ADCs)

Source: www.maximintegrated.com/en/app-notes/index.mvp/id/1080

DC-DC converters



$$L(s) = \frac{a}{sC_cR_c}\frac{V_s}{V_r}\frac{1}{s^2LC + sL/R + 1}$$

Steady state $V_o = V_{ref}/a$

- DC-DC buck converter
- Average model from duty cycle to the output
- Voltage regulation loop and its stability

Acknowledgments: Army of TAs